REMARKS

Claims 1-29 are pending in the present application. In the Office Action, claim 11 was rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In particular, the Examiner alleges that "the second I/O bus" set forth in claim 11 lacks antecedent basis. Claim 11 has been amended solely to correct a typographical error. Applicants submit that claim 11 is definite and request that the Examiner's rejection of claim 11 under 35 USC 112, second paragraph, be withdrawn.

In the Office Action, claims 1-4, 10-16, 18-20, 23-26, and 28-29 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Chang, et al. (U.S. Patent No. 6,286,097). Claims 5-9, 17, 21-22, and 27 were rejected under 35 U.S.C. 103(a) as allegedly being obvious over Chang in view of Davis (U.S. Patent No. 5,844,986). The Examiner's rejections are respectfully traversed.

Claims 1, 14, 20, 23, and 24 set forth a processor, a device coupled to the processor, and a memory selectably coupled to the device and the processor. Claims 1, 14, 20, 23, and 24 also set forth a switching mechanism coupled between the memory and each of the processor and the device, wherein the switching mechanism includes a first state providing access from the processor to the memory and a second state providing access from the device to the memory. In claim 1, the device is a bridge.

Chang describes a computer chipset 320 that is coupled to a main processor 310, a peripheral device 340, and a Read Only Memory (ROM) 350. The main processor 310 is coupled to a main control circuit 321 on the chipset 320. The main control circuit 321 is coupled to a peripheral control circuit 322 and a booting control circuit 323. The peripheral control

circuit 322 and the booting control circuit 323 provide inputs A and B, respectively, to a switching circuit 325, which provides one of the inputs A or B as an output Y to the peripheral device 340 or the ROM 350 based upon a booting enable signal (BTEN) provided to an input/output port S of the switching circuit 325 by the booting control circuit 323. When the booting enable signal (BTEN) is activated, the switching circuit 325 connects the booting control circuit 323 to the ROM 350. When the booting enable signal (BTEN) is not activated, the switching circuit 325 connects the peripheral control circuit 322 to the peripheral device 340.

However, Applicants respectfully submit that Chang does not describe or suggest a switching mechanism that provides a first state providing access from a processor to a memory and a second state providing access from the device to the memory. Furthermore, with particular regard to independent claim 1, Applicants respectfully submit that the peripheral control circuit 322 described by Chang is not a bridge.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Chang and request that the Examiner's rejections of claims 1-4, 10-16, 18-20, 23-26, and 28-29 under 35 U.S.C. 102(e) be withdrawn.

Moreover, it is respectfully submitted that the present invention is not obvious in view of Chang or Davis, either alone or in combination. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Chang fails to teach or suggest a switching mechanism that provides a first state providing access from a processor to a memory and a second state providing access from the device to the memory, as set forth in independent claims 1, 14, 20, 23, and 24. The Examiner relies upon

Davis to describe a secure BIOS ROM housed within a crypto-processor. Davis does not, however, remedy the fundamental deficiencies in Chang.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over Chang in view of Davis. Applicants respectfully request that the Examiner's rejections of claims 5-9, 17, 21-22, and 27 under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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